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09/148,606	09/04/98	YONEDA	K 5586D-6885

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WM02/1120

EXAMINER

ZAMANI, A

ART UNIT

PAPER NUMBER

2674

DATE MAILED:

11/20/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/148,606

Applicant(s)
Yoneda et al.

Examiner
All Zamani

Group Art Unit
2674



☒ Responsive to communication(s) filed on Sep 5, 2000

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-22 is/are pending in the application

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-8, 10-13, 15, 16, and 19 is/are rejected.

☒ Claim(s) 9, 14, 17, 18, and 20-22 is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipate by Kato et al. (US Pat. No. 5,589,406)

3. In regard to claims 1-4, Kato et al disclose a semiconductor device include a TFT substrate (100) for a liquid crystal display device wherein a pixel region (5), row driver circuit (6) and column driver circuit 7 are formed on a glass substrate (col. 7, lines 56-59). In the pixel region 5, switching transistors such as TFTs having polycrystalline semiconductor channels, pixel electrode lines (gate bus lines) are arranged in a matrix form. The semiconductor layers (channels, sources and drains) of these TFT circuits are composed of polycrystalline Si which is formed by beam-annealing (col. 8, line 23). In beam-annealing the glass substrate over a range having a width (fig. 4), the structure of each of the row driver circuit (6) is so formed that the transistors in the row driver circuit (6) are disposed on the same line as the transistors for picture display (col. 8, lines 29-35), in some or all of said semiconductor elements, a channel width of a channel region formed in a semiconductor layer to which laser annealing is applied is larger than a channel length thereof, see examples 2 and 3, cols. 9 and 10 which all function as claimed.

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4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5- 8, 10-13, 15-16, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al in view of Koyama et al (US Pat. No. 6,037,924).

6. In regard to claims 5-8, 10-13, 15-16 and 19, Kato et al is discussed above. Kato et al show all the above claimed limitations except for the "plurality of second thin-film transistors constituting a scanning drive circuit for scanning said plurality of first thin-film transistors". However, Koyama et al disclose a matrix type liquid-crystal display unit in which a pixel is arranged at each intersection of a matrix which is made up of signal lines 1 and scanning lines 2 (gate line), which is arranged in parallel to a subject row, being connected to gate electrode of thin-film transistor 4 of the subject row, and a column in the matrix is defined by the signal line 1 (source line), which is arranged in parallel to a subject row being connected to a source (or drain) electrode of the thin-film transistor (4) (column 1, lines 14-35) and as reference (Fig. 7), n-type TFT, first an island-like region (701) made of intrinsic polysilicon is formed. Then, a gate insulating film is formed, and a gate electrode film is formed on the gate insulating film. The gate electrode film is etched to form a gate electrode (702). Therefore, the island-like region (701) is doped with n-type impurities to form an n-type source/drain region (703). when a negative voltage is applied to the p-type layer (906), a depletion layer (907) defined between the channel

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(905) which is an n-type layer of the channel p-type layer (906) formed under the channel (905) spreads and serves to suppress the channel (905), thereby making it difficult to allow a current to flow into the channel (905). As a result, the threshold value becomes large. On the other hand, when a positive voltage is applied to the p-type layer (906), the depletion layer (907) is narrowed to make the current readily flow thereinto. As a result, the threshold value is reduced. Thus it would have been obvious to one of ordinary skill in the art to utilize the noted teaching of Koyama et al with the display device of Kato et al because both references are related to liquid-crystal display for controlling a timing for rewriting image data in each pixel, so as to provide a high-resolution animation in a large image plane (Figs. 1-7, cols 1, 3 and 7).

7. Claims 9, 14, 17, 18, 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Masumo et al, Sakamoto and Kubota et al are made of record to show various types of polycrystalline semiconductor (TFTs) and method of making TFT display.

Response to Arguments

9. Applicant's arguments filed on 09-05-00 with respect to claims 1-22 have been fully considered but they are not persuasive.

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a. On page 2, Applicant's argues that Kato does not teach or suggest that the channel width direction of the driver transistors differs from the side directions of the substrate of the display device or from the longitudinal and/or short axial directions of the laser beam used to anneal the display device. However, the examiner contends that Kato does teach the channel width direction of the driver transistors differs from the side directions of the substrate of the display device or from the longitudinal and/or short axial directions of the laser beam used to anneal the display device (col. 5, lines 26-53) and (Fig. 7, col. 7, lines 16-51).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ali Zamani whose telephone number is (703) 308-6414. The examiner can normally be reached on Monday through Friday from 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe, can be reached on (703) 305-4709. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Ali Zamani

November 16, 2000

A handwritten signature in black ink, appearing to read 'R. Hjerpe', with a stylized flourish at the end.

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600